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Four-phase Logic Circuits using Integrated m-o-s Transistors

R. J. HATT, A. E. JACKETS and D. B. JARVIS
Associated Semiconductor Manufacturers Ltd

The operating principles and design of four-phase m-o-s transistor logic are described by considering the shift register, combinational logic, negators and staticisors. The clock generator requirements are also described and a design for a four-phase generator is given. High noise immunity interface circuits are considered together with some basic layout designs.

INTRODUCTION

Integrated circuits using m-o-s transistors are now well established. They feature a high packing density, very low power dissipation, relatively high noise margin, and in addition, circuits may be customised since a common production process can be used to fabricate a variety of circuits; only new masks and test schedules are required for circuit changes.

To date, most of the integrated circuits using p-channel transistors which have become commercially available have utilised a two-phase clocking system. Although they are attractive for some applications, circuits of this type have the drawback that the load and logic transistors can conduct simultaneously. So a relatively large logic transistor is required to obtain a low '0' level. This means that the logic transistors must consume a relatively large area on the chip, particularly if the logic system uses m-o-s transistors connected in series. However, circuits have been introduced recently which employ a four-phase clocking system. In these circuits the load and logic transistors do not conduct simultaneously so that the transistors can be of a similar size and of minimum dimensions. In addition, the power dissipation is reduced and the maximum clock operating frequency is increased.

In four-phase dynamic circuitry the node capacitance is precharged by one phase (ϕ_1) and discharged (or not) by the second phase (ϕ_2) according to the logic input. As in the two-phase system there are two nodes per bit, so a total of four phases is required. The only power consumed is due to the energy lost when the voltage across a capacitance is changed; this results in a power dissipation of about 100µW per stage at 1MHz. Probably the main disadvantage of the system is the generation of the four-phase clock pulses, but it is anticipated that in many cases, particularly where low frequency operation is required, two of these phases can be generated on-the-chip so that only a two-phase clock supply is necessary. In many cases a d.c. supply to the chip is not required.

The operating principles of four-phase m-o-s transistor logic are described by considering the shift register, combinational logic, negators and staticisors. The clock generator requirements are also described and a design for a four-phase generator is given. Staticisor and high noise immunity circuits are considered, together with some basic layout designs.

FOUR-PHASE LOGIC CIRCUITS AND THEIR OPERATION

The operating principles of the basic four-phase logic circuits are considered in turn. Detailed performance calculations are not carried out but are considered later in conjunction with a specific layout.

Shift Register

Fig. 1* shows the circuit diagram, logic symbol and waveforms of a four-phase shift register circuit. It will be seen that each stage of the register consists of six transistors.

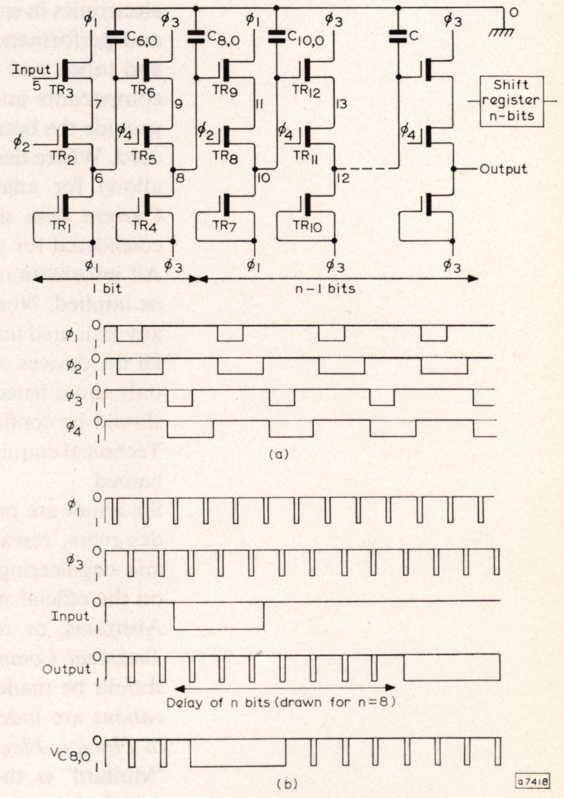

Fig. 1—Four-phase shift register

(a) Clock waveforms and circuit diagram
(b) Input and output waveforms

The node capacitances $C_{6,0}$ and $C_{8,0}$ play an important part in the circuit operation and are composed of the diffusion capacitance, the interconnection capacitance and the gate-to-substrate capacitance of TR$_6$ and TR$_9$ respectively. The leakage current of this capacitance to the substrate is very small since it is composed mainly of the diffusion leakage current, which is of the order of 1nA. Thus the node capacitance can be used as a store for long periods (page 275). A feature of this circuit is that the transistors can all be of the minimum size determined by the fabrication procedures.

During ϕ_1 time, $C_{6,0}$ is precharged by TR$_1$ and discharged, or not discharged according to the state of the input, by TR$_2$ and TR$_3$ just after ϕ_1 has returned to earth potential. Similarly $C_{8,0}$ is precharged during ϕ_3 time by TR$_4$ and discharged, or not, by TR$_5$ and TR$_6$. If the input is at earth potential then $C_{6,0}$ which is precharged during ϕ_1 time, will not be discharged when ϕ_1 returns to earth potential as TR$_3$ cannot conduct. During ϕ_3 time $C_{8,0}$ is precharged but when ϕ_3 returns to earth potential TR$_5$ and TR$_6$ conduct to discharge it. So when the input is at earth potential $C_{6,0}$, $C_{10,0}$ . . . are charged and $C_{8,0}$, $C_{12,0}$ . . . are discharged. If the input now goes to '1' (a negative voltage greater than the threshold voltage) as shown in Fig. 1, then $C_{6,0}$ is discharged by TR$_2$ and TR$_3$ just after the end of ϕ_1 time. This means that $C_{8,0}$ which is charged during ϕ_3 time, remains charged at the end of ϕ_3 time since TR$_6$ cannot conduct. Thus the output from the first bit is similar to the input but is delayed by one clock period. Similarly for an n-bit shift register the output is delayed by n clock periods as shown in Fig. 1.

It will be seen that the node capacitances are charged by ϕ_1 and ϕ_3 and discharged by ϕ_2 and ϕ_4. The information on $C_{6,0}$ is read at the end of ϕ_3 time. The source of TR$_3$ is connected to ϕ_1 to prevent TR$_3$ conducting (and consuming power) during ϕ_1 time. A more detailed analysis of this circuit, including the effects of the gate-to-drain and gate-to-source feedback capacitances, is given in *Effect of Feedback Capacitance* (page 271).

When the output of the register is at '1' the output waveform is a d.c. voltage given approximately by the peak clock voltage minus the threshold voltage. When the output is at '0' (a voltage less than the threshold voltage) the output level is pulsed during ϕ_3 time as shown in Fig. 1. This waveform is a consequence of the operating principles of this type of logic, and a staticisor circuit is required if a steady '0' level output is required.

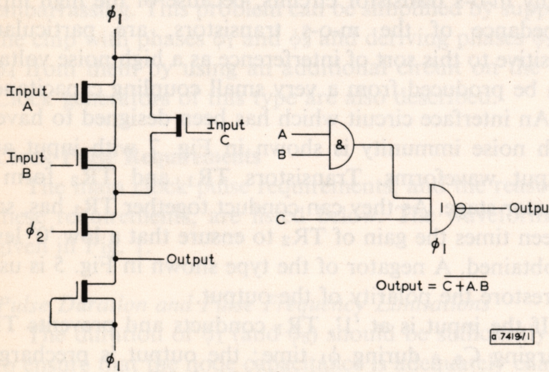

Fig. 2—Combinational logic

Combinational Logic

Fig. 2 shows how logic functions can be performed. The circuit is similar to the half-shift register stage shown in Fig. 1 but with TR$_3$ replaced by additional logic transistors. In this case the operation is similar to that of a shift register but the condition for the discharge of the node capacitance is determined by the additional logic transistors. As a further example Fig. 3 shows a bistable circuit.

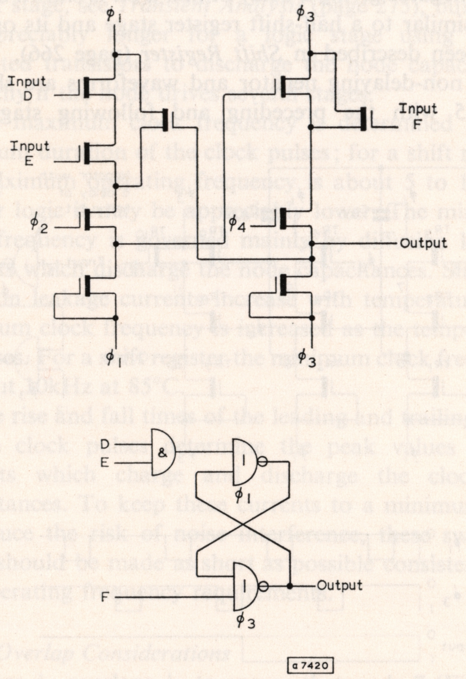

Fig. 3—Bistable circuit

All the transistors in these circuits can have similar dimensions. However, if high frequency operation is required, then it is important to calculate the

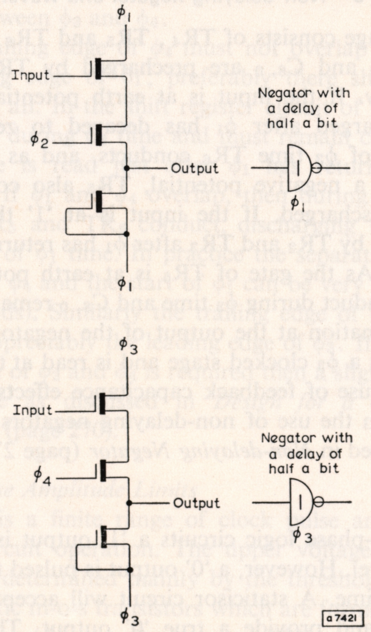
ϕ1
Input
ϕ2
Output
ϕ1
Negator with a delay of half a bit
1
ϕ1
ϕ3
Input
ϕ4
Output
ϕ3
Negator with a delay of half a bit
1
ϕ3
a7421

Fig. 4—Negator with delay of half a bit

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*Note: In all figures the substrate connection to all transistors has been omitted for simplicity.

probable maximum operating frequency for the layout; this topic is considered further in *Design Methods* (page 275).

As the input resistance of an m-o-s transistor is very high, about $10^{15}\Omega$, an output node can drive many gates, limited only by the deterioration of the switching time, due to the addition of the gate capacitances to the node capacitance.

Negator

A negator giving a delay of half a bit is shown in Fig. 4. It is similar to a half-shift register stage and its operation has been described in *Shift Register* (page 266).

A non-delaying negator and waveforms are shown in Fig. 5 with the preceding and following stages. The negator stage consists of TR_4, TR_5 and TR_6. During ϕ_1 time, $C_{6,0}$ and $C_{8,0}$ are precharged by TR_1 and TR_4 respectively. If the input is at earth potential $C_{6,0}$ will remain charged after ϕ_1 has decayed to zero. At the beginning of ϕ_3 time TR_6 conducts, and as the gate of TR_5 is at a negative potential, TR_5 also conducts and $C_{8,0}$ is discharged. If the input is at '1' then $C_{6,0}$ is discharged by TR_2 and TR_3 after ϕ_1 has returned to earth potential. As the gate of TR_5 is at earth potential, TR_5 cannot conduct during ϕ_3 time and $C_{8,0}$ remains charged. The information at the output of the negator is suitable for driving a ϕ_3 clocked stage and is read at the end of ϕ_3 time. Because of feedback capacitance effects, care must be taken in the use of non-delaying negators. This topic is considered in *Non-delaying Negator* (page 272).

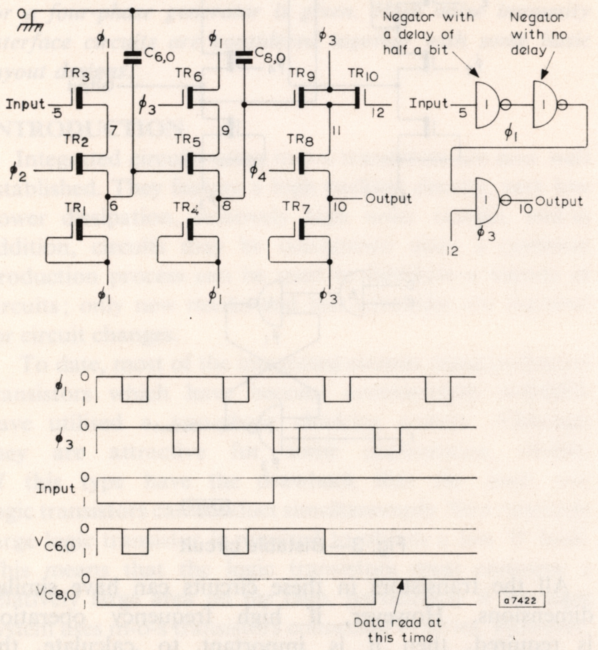

Fig. 5—Non-delaying negator and waveforms

Staticisor

In four-phase logic circuits a '1' output is a constant voltage level. However, a '0' output is pulsed to '1' during ϕ_1 or ϕ_3 time. A staticisor circuit will accept the pulsed '0' input and provide a true '0' output. The '1' input signal is unchanged.

Fig. 6 shows a circuit which realises these requirements. In this arrangement TR_1 has a much higher gain than TR_2 so that when TR_1 is ON its drain-to-source voltage is less than the threshold voltage. TR_4 is also larger than a normal logic transistor to enable a reasonably large output current, say a few hundred microamperes, to be obtained. The relative gain factors are indicated for a typical case; β being the gain factor of a normal logic transistor. If the circuit is fed from a '1' input TR_1 will always present a low resistance to prevent $C_{7,0}$ being charged, and I_o is zero. With a '0' input ϕ_1 charges $C_{7,0}$ and an output current I_o flows. When the '0' level at the input is clocked to '1' during ϕ_3 time TR_1 cannot discharge $C_{7,0}$ since TR_3 is non-conducting. The output current can be used to drive an n-p-n bipolar transistor as shown.

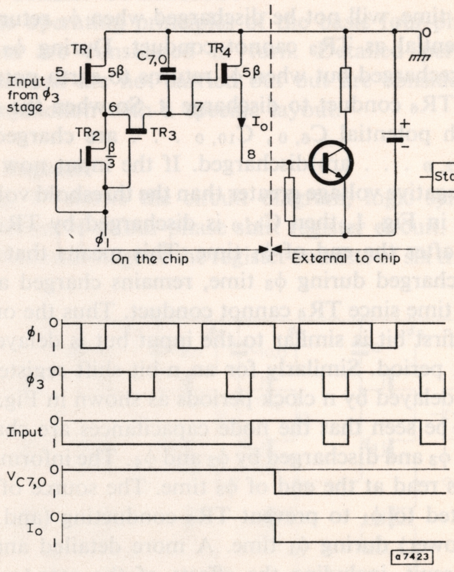

Fig. 6—Staticisor and waveforms
(β is the gain factor of a minimum area m-o-s transistor. The gain factors shown are for guidance only.)

Interface Circuits

When a system is composed of more than one package the design of interface circuits to connect the packages must be considered. The interface circuit should not reduce the transient response to an unacceptable level and must not be susceptible to noise that is generated by stray capacitive coupling to the interconnecting leads. Many m-o-s transistor circuits, because of the high input impedance of the m-o-s transistors, are particularly sensitive to this sort of interference as a high noise voltage can be produced from a very small coupling capacitance.

An interface circuit which has been designed to have a high noise immunity is shown in Fig. 7 with input and output waveforms. Transistors TR_1 and TR_2 form a negator stage. As they can conduct together TR_1 has, say, fifteen times the gain of TR_2 to ensure that a low '0' level is obtained. A negator of the type shown in Fig. 5 is used to restore the polarity of the output.

If the input is at '1', TR_1 conducts and prevents TR_2 charging $C_{6,0}$ during ϕ_1 time; the output is precharged during ϕ_3 time by TR_5 and remains charged as TR_4 is held off. To produce a malfunction the noise must develop a voltage greater than the threshold voltage across the ON resistance (about 3kΩ) of TR_1.

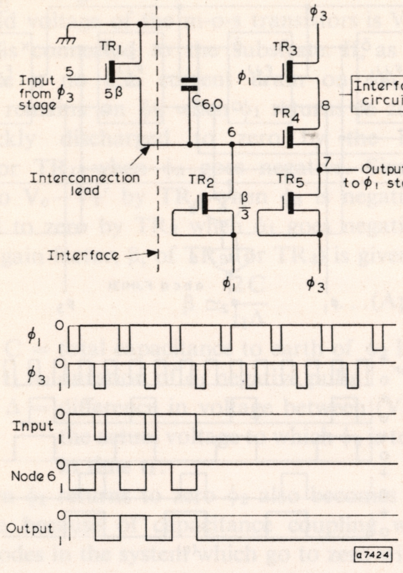

Fig. 7—High noise immunity interface circuit and waveforms
(β is the gain factor of a minimum area m-o-s transistor. The gain factors shown are for guidance only.)

If the input signal is at '0', TR_1 is held off, and during ϕ_1 time TR_2 takes the gate of TR_4 to a negative potential. The output node 7, which has been precharged during ϕ_3 time, is discharged at the beginning of ϕ_1 time as in a normal negator stage, hence the output cannot drive another non-delaying negator but can be driven from one. A noise signal which tends to take the interconnection negative can only prematurely discharge the output node 7 and this will not influence the circuit operation. A positive noise signal must keep the interconnection at a potential less negative than the threshold voltage during ϕ_1 time when TR_2 is ON if it is to cause the circuit to malfunction.

CLOCK PULSE GENERATION

One of the features of four-phase logic is that the clock generation requirements are relatively easy to meet. Nevertheless, it is important to fulfil certain basic requirements and these are discussed in this section. A design for a four-phase clock generator is also given.

In some cases the generation of four phases may be embarrassing. This problem can be simplified by supplying the chip with phases ϕ_1 and ϕ_3 and deriving phases ϕ_2 and ϕ_4 from them by using an additional circuit on the chip. Clock generators of this type are also described.

Clock Pulse Requirements

The main clock pulse requirements, and the reason for these requirements, are listed below. The waveforms are given in Fig. 1.

Pulse Duration and Pulse Frequency Limitations

The duration of ϕ_1 (and ϕ_3) should be sufficiently long to ensure that the node capacitance is adequately charged. A calculation of this time is given in *Transient Analysis* (page 275) for a specific layout; typically this capacitance is adequately charged after about 30ns for a shift register stage. Hence, this value represents the minimum duration of ϕ_1, but if a low clock frequency is permissible, ϕ_1 can be much longer than this, say many microseconds. This simplifies the generation of ϕ_1 and ϕ_3.

The period for which ϕ_2 continues after ϕ_1 has fallen to zero is determined by the discharge time of the node capacitance. Typically this time is about 20ns for a shift register stage, see *Transient Analysis* (page 275), but it can be appreciably longer for a logic stage using series-connected transistors to discharge the node capacitance, especially if the node drives several stages.

The maximum clock frequency is determined by the minimum duration of the clock pulses; for a shift register the maximum operating frequency is about 5 to 10MHz but for logic it may be appreciably lower. The minimum clock frequency is governed mainly by diffusion leakage currents which discharge the node capacitances. Since the diffusion leakage currents increase with temperature, the minimum clock frequency is increased as the temperature increases. For a shift register the minimum clock frequency is about 10kHz at 85°C.

The rise and fall times of the leading and trailing edges of the clock pulses determine the peak values of the currents which charge and discharge the clock line capacitances. To keep these currents to a minimum, and to reduce the risk of noise interference, these switching times should be made as short as possible consistent with the operating frequency requirements.

Pulse Overlap Considerations

Phase ϕ_2 overlaps ϕ_1 to ensure that node 7 (Fig. 1) is charged during ϕ_1 time. If node 7 is not charged during ϕ_1 time a loss of charge on node 6 occurs when ϕ_1 ceases; this loss of charge is due to charge sharing between nodes 6 and 7. Usually it simplifies the clock generator circuit if ϕ_2 and ϕ_1 commence at the same time. A similar overlap occurs between ϕ_3 and ϕ_4.

The trailing edge of ϕ_4 must not overlap appreciably the leading edge of ϕ_1; preferably there should be no overlap at all. In the shift register circuit of Fig. 1, $C_{8,0}$ is charged during ϕ_3 time and must remain charged until its voltage is read just after ϕ_1 has returned to zero potential. If ϕ_1 and ϕ_4 overlap, then during the overlap period TR_5 and TR_6 conduct, discharging $C_{8,0}$ at the beginning of ϕ_1 time. In practice the separation between the end of ϕ_4 and the start of ϕ_1 can be very short (a few nanoseconds). Similarly the trailing edge of ϕ_2 must not overlap appreciably the leading edge of ϕ_3. If on-the-chip generation of ϕ_2 and ϕ_4 is required then a slight overlap is permissible as discussed in *Design for a Clock Pulse Generator* (page 270).

Clock Pulse Amplitude Limits

There is a finite range of clock pulse amplitude for correct circuit operation. The upper voltage limit of ϕ_1 and ϕ_3 is determined mainly by the threshold voltage of the parasitic m-o-s transistors which are formed under the thick oxide (*Layout Design* page 273) or the junction voltage rating if this is lower. The threshold voltage of the thin oxide transistors determines the minimum operating voltage, which must be equal to at least twice the threshold voltage plus a volt or two to turn on the logic transistor. If high frequency operation is required a larger drive voltage is required. In Fig. 1 the amplitude of ϕ_1 must be sufficient to charge $C_{6,0}$ via TR_1 to a voltage greater than the threshold voltage of TR_6; thus a voltage a little greater than the sum of the threshold voltages of TR_1 and TR_6 is required. When calculating this voltage it should be remembered that the threshold voltage of TR_1 is increased because its source is reverse biased with respect to the substrate.

The maximum voltage amplitude of ϕ_2 and ϕ_4 is governed, as in the case of ϕ_1 and ϕ_3, by the formation of parasitic channels. However, the minimum voltage of ϕ_2 must be sufficient to turn on TR_2; this means a voltage slightly greater than the threshold voltage of TR_2, which is again increased by source-substrate bias. Thus the minimum voltage of ϕ_2 is less than the minimum voltage of ϕ_1 by a voltage approximately equal to the threshold voltage.

In practice it is often convenient to have equal amplitudes for all the clock phases. However, when on-the-chip generation of ϕ_2 and ϕ_4 is required it is necessary to make the amplitude of ϕ_2 and ϕ_4 less than that of ϕ_1 and ϕ_3 and this is permissible if the above conditions are fulfilled. Typically the clock operating range at 50kHz is 14 to 28V but this range may be modified at extreme clock frequencies. The minimum voltage amplitude of ϕ_2 and ϕ_4 is about 10V. A lowered voltage for ϕ_2 and ϕ_4 after ϕ_1 and ϕ_3 time is advantageous in reducing the effects of feedback and crossover capacitances.

Design for a Clock Pulse Generator

An arrangement for a simple clock pulse generator for testing breadboard circuits is given in Fig. 8. It uses four integrated circuit packages to derive the four phases from a single pulse train. These packages drive four output stages which generate the clock waveforms. Four JK flip-flops are connected as a ring counter and a pattern with a 1 : 3 mark-space ratio circulates. To inhibit other patterns the three J inputs of the first stage are connected as shown in the figure. The trigger voltage together with gates a and c are used to reduce the width of ϕ_2 and ϕ_4 by an amount equal to the trigger pulse duration; this prevents ϕ_2 and ϕ_4 from overlapping ϕ_3 and ϕ_1 respectively. Gates b and d are used to form phases ϕ_2 and ϕ_4.

Two output stages are shown. The two-transistor circuit is suitable when one terminal of the clock pulse generator is at earth potential; the simple circuit is to be preferred when the clock pulse generator has a transformer-fed output. For operation above about 2MHz the circuit impedances may have to be reduced.

Internal Generation of ϕ_2 and ϕ_4

A possible disadvantage of four-phase circuits is the need to generate four clocks and connect them to the chips. However, this disadvantage can be largely avoided by generating ϕ_2 and ϕ_4 internally on each chip from ϕ_1 and ϕ_3.

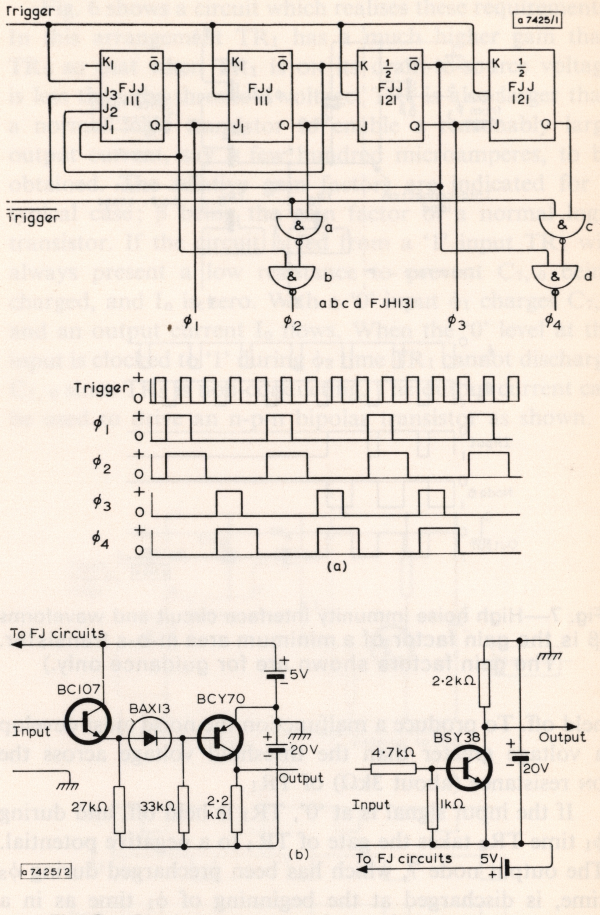

Fig. 8—Clock generator and waveforms
(a) Four-phase clock generator and waveforms
(b) Output stages

A circuit for doing this simply is shown in Fig. 9. When ϕ_1 goes negative to a voltage V_c the ϕ_2 output is charged negatively by TR_2 to a value $V_c - V_T'$, where V_T' is the threshold voltage of TR_2 with its source at $V_c - V_T'$. The threshold voltage of the m-o-s transistors is V_T when the source is connected to the substrate. If, as is normally so, there is no d.c. current drain on ϕ_2, a negative voltage remains on ϕ_2 when ϕ_1 returns to zero. Line ϕ_2 is quickly discharged to zero by the large m-o-s transistor TR_1 when ϕ_3 goes negative. Similarly ϕ_4 is taken to $V_c - V_T'$ by TR_4 when ϕ_3 is negative and discharged to zero by TR_3 when ϕ_1 goes negative.

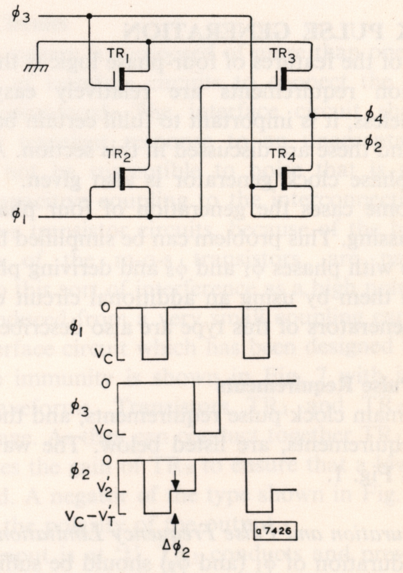

Fig. 9—Circuit for generating ϕ_2 and ϕ_4 internally on the chip from ϕ_1 and ϕ_3

The gain factor, β, of TR_2 (or TR_4) is given by:

$$\beta \simeq \frac{2C}{t_1\Delta} \quad \ldots\text{(Appendix 1A)}$$

where: C = total capacitance to earth of ϕ_2 line
t_1 = duration of ϕ_1 negative pulse
Δ = difference in voltage between $(V_c - V_T')$ and the actual voltage to which ϕ_2 is to be charged in time t_1.

When ϕ_1 returns to zero ϕ_2 also becomes slightly less negative because of capacitance coupling with ϕ_1 and other nodes in the system which go to zero with ϕ_1. Most incidental coupling can be reduced by layout design but some coupling is fundamental to the basic operation. In Fig. 10, if node 6 output is a logic '1', then, when ϕ_1 returns to zero after its negative pulse, nodes 8 and 9 go to zero and are coupled to ϕ_2 by the feedback capacitances of TR_9. This effect does not occur when the output of node 6 is a logic '0'. Hence, the final voltage of ϕ_2 depends on the pattern of logic signals being propagated through the several stages driven with ϕ_2. The worst case is when all nodes 6 have an output of '1'.

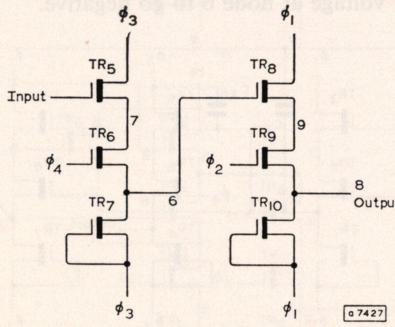

Fig. 10—Single shift register stage

Initially node 8 is at $V_c - V_T'$ and node 9 is at $V_c - V_T - V_T''$, where V_T'' is the threshold voltage of TR_9 when its source is at $V_c - V_T - V_T''$. Hence the voltage, V_2', of ϕ_2 after ϕ_1 goes to zero is given by:

$$V_2' = \frac{C_s(V_c - V_T') + C_{gs(ON)}(V_T'')}{C_s + C_{gs(ON)} + C_{gd}}$$

where: C_s = total ϕ_2 line capacitance to earth apart from $C_{gs(ON)} + C_{gd}$
$C_{gs(ON)}$ = total gate-source capacitance of all transistors TR_9 whose node 9 goes to zero
C_{gd} = total gate-drain capacitance of all transistors TR_9 whose node 8 goes to zero.

Some reduction in ϕ_2 is beneficial but if V_2' is too small the maximum speed may be reduced. A typical compromise is to make C_s and $(C_{gs(ON)} + C_{gd})$ approximately equal.

The gain factor of TR_1 (and similarly TR_3) is determined by the overlap allowable between ϕ_2 and ϕ_3. In Fig. 10, if node 8 is storing a logic '1', when ϕ_3 goes negative TR_8 is turned on by TR_7 and so node 9 discharges to zero. At the same time ϕ_2 is discharged to zero by TR_1 in Fig. 9. These two voltage transients are applied to the source and gate of TR_9 respectively, and must be so arranged that TR_9 does not turn on, otherwise node 8 would be discharged towards zero.

A computer programme has been written for calculating the minimum gain factor of TR_1 according to the simple equivalent circuit shown in Fig. 11. Starting from a large value, β is reduced until, at any time during the transient, $|V_2 - V_9| = |V_T|$. A typical example is as follows:

$V_c = -30V$, $V_2 \text{ (initial)} = -24V$, $V_T = -3V$,
$C_{ST} = 8pF$, $C_{XT} = 120fF$, $C_{YT} = 40fF$,
$\beta_2 = 6\mu A/V^2$, $\beta_3 = 6\mu A/V^2$
(where fF = femtofarad = $10^{-15}F$)

Calculated values are shown in the table:

t_R(ns)	min $\beta_1(\mu A/V^2)$
1	200
10	160
100	120
1000	60
3000	34

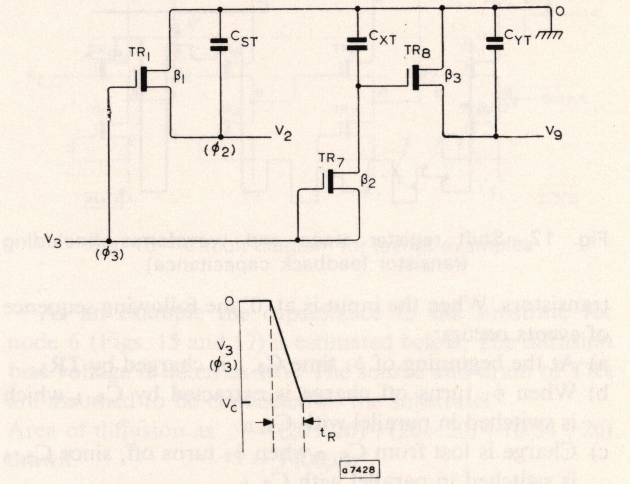

Fig. 11—Simple equivalent circuit used for the calculation of the minimum value of β_1

CIRCUIT DESIGN PRINCIPLES AND CIRCUIT CONFIGURATION

A shift register stage is used to illustrate circuit design principles, including the effect of feedback capacitances. Then a number of topics are discussed which have proved to be important in the design of logic systems.

Effect of Feedback Capacitance

As the gate of a transistor must overlap the source and drain diffused regions, capacitances exist between gate and source and gate and drain. The gate-to-source capacitance has a value approximately equal to one half the gate-to-substrate capacitance and has a considerable influence on the node voltage.

Fig. 12 shows the circuit diagram of a shift register stage including the important feedback capacitances, with waveforms obtained by simulating the circuit with discrete

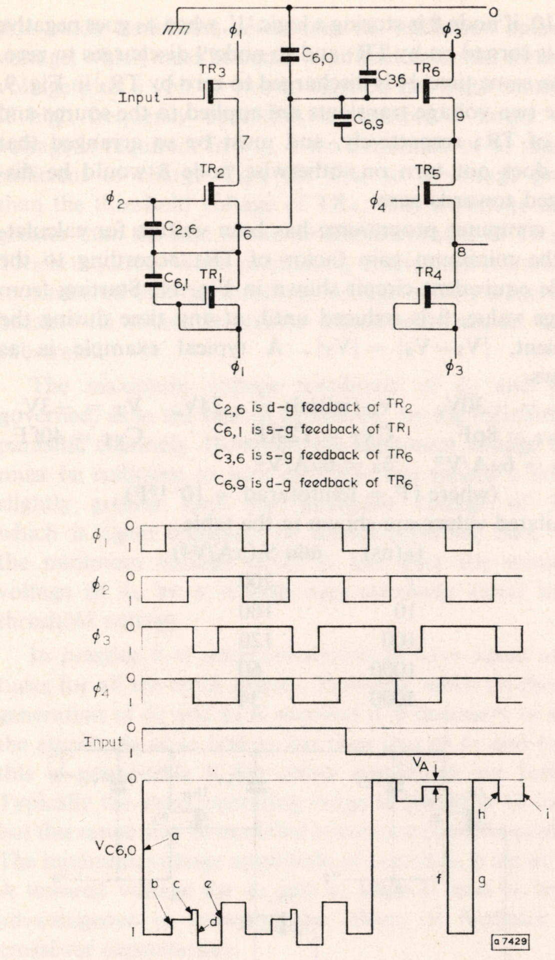
Input
TR3
TR2
TR1
TR6
TR5
TR4
$C_{6,0}$
$C_{3,6}$
$C_{6,9}$
$C_{2,6}$
$C_{6,1}$
ϕ_3
ϕ_2
ϕ_4
ϕ_1
$C_{2,6}$ is d–g feedback of TR_2
$C_{6,1}$ is s–g feedback of TR_1
$C_{3,6}$ is s–g feedback of TR_6
$C_{6,9}$ is d–g feedback of TR_6
V_A
$V_{C6,0}$
a b c d e f g h i
a7429

Fig. 12—Shift register stage and waveforms (including transistor feedback capacitance)

transistors. When the input is at ‘0’ the following sequence of events occurs:

a) At the beginning of ϕ_1 time $C_{6,0}$ is charged by TR_1.
b) When ϕ_1 turns off charge is extracted by $C_{6,1}$ which is switched in parallel with $C_{6,0}$.
c) Charge is lost from $C_{6,0}$ when ϕ_2 turns off, since $C_{2,6}$ is switched in parallel with $C_{6,0}$.
d) Charge is gained by $C_{6,0}$ when ϕ_3 turns on, via $C_{3,6}$ and $C_{6,9}$.
e) Charge is lost by $C_{6,0}$ when ϕ_3 turns off, via $C_{6,9}$ and $C_{3,6}$.

The charge remaining on $C_{6,0}$ is now read immediately after ϕ_3 has turned off. This voltage must be large enough to drive the next stage.

An additional factor not considered in Fig. 12 is the diffusion leakage current which tends to discharge $C_{6,0}$. The magnitude of this current increases as the temperature increases, and is an important factor when low frequency operation is required.

When the input is at ‘1’ we have:

f) At the beginning of ϕ_1 time $C_{6,0}$ is charged by TR_1.
g) Just after ϕ_1 has returned to earth potential $C_{6,0}$ is discharged by TR_2 and TR_3.
h) When ϕ_3 conducts charge is added to $C_{6,0}$ by $C_{6,9}$ and $C_{3,6}$.
i) When ϕ_3 turns off charge is subtracted by $C_{3,6}$.

The voltage remaining on $C_{6,0}$ is now read at the end of ϕ_3 time. This voltage must be less than the threshold voltage to ensure the next stage does not conduct.

For a particular layout the node voltage can be estimated at the time it is read. This is done by calculating the voltage to which $C_{6,0}$ is initially charged and then the charge lost is calculated for each transient. For a standard shift register circuit a calculation of this type is probably not necessary because the charge lost is relatively small. However, in a complex logic system, in addition to charge lost due to transistor feedback capacitance, charge is also lost due to crossover capacitances, especially when one node feeds a distant point in the circuit. A method for estimating the charge lost in this case for critical nodes is presented on page 275.

Non-Delaying Negator

A non-delaying negator should not be fed directly from a stage that drives another circuit. The circuit diagram of a simple arrangement to illustrate this topic is given in Fig. 13a. If the input is at ‘1’ $C_{6,0}$ will charge during ϕ_1 time and discharge at the end of ϕ_1 time via TR_2 and TR_3. Also charged by ϕ_1, is $C_{10,0}$. When ϕ_3 goes negative, the source-to-gate capacitance $C_{3,6}$ of TR_6 causes the voltage at node 6 to go negative.

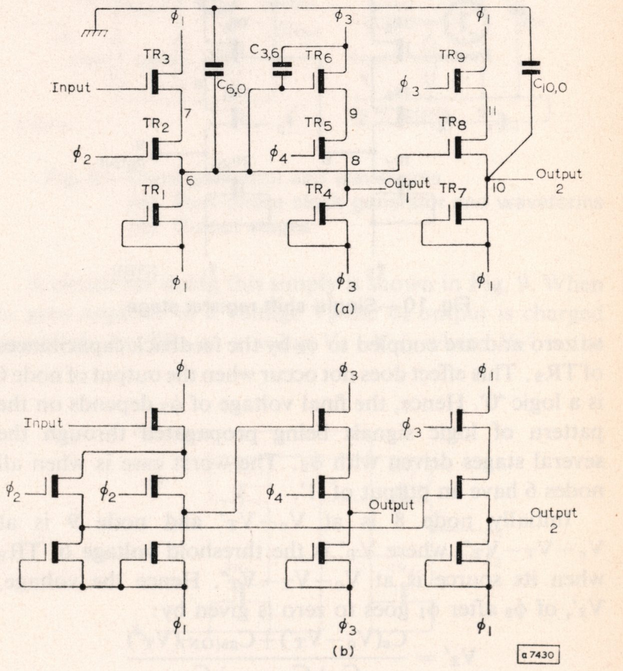

Fig. 13—*(a)* Circuit showing a negator and a ϕ_3 stage driven from a ϕ_1 stage (Note: this does not function but is shown to illustrate a problem discussed in the text)
(b) Split output circuit

In practice, this feedback voltage can exceed the magnitude of the threshold voltage, and this results in TR_8 turning on at the beginning of ϕ_3 time. So the information stored on $C_{10,0}$ is destroyed at the beginning of ϕ_3 time due to TR_8 and TR_9 conducting together. This problem is eliminated by splitting the output circuits of the driving stage as shown in Fig. 13b.

Sneak Paths

Fig. 14a shows a simple logic circuit. As the gates of TR_4 and TR_9 are supplied from a common input A and must conduct together it would seem reasonable to use one transistor in place of TR_4 and TR_9 as shown in Fig. 14b. However, a sneak path can occur in this simplified circuit as follows. If B, C and D are at ‘1’ and A is at ‘0’, TR_8 can conduct via TR_3 and TR_5 and node 9 is discharged. This should not happen and cannot occur in the circuit of Fig. 14a. Hence if the circuit is simplified it should be carefully examined for sneak paths.

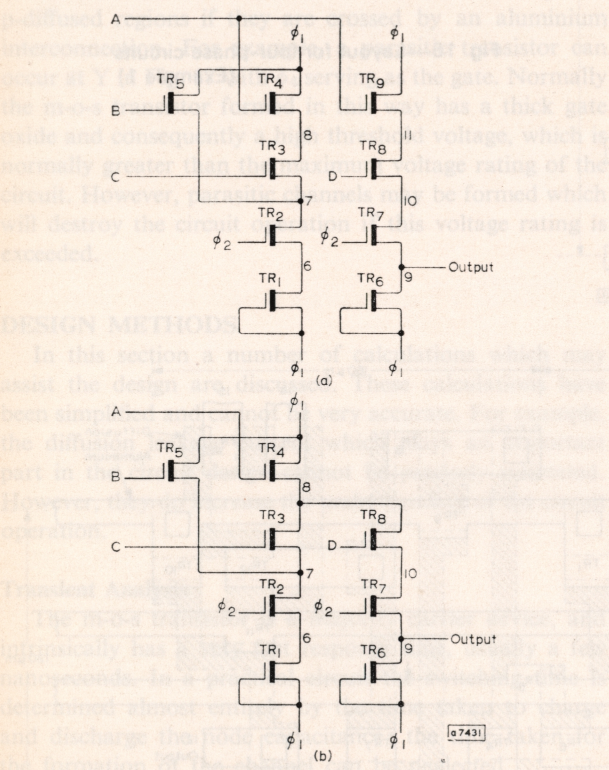

Fig. 14—Circuits illustrating sneak paths
(a) Simple logic circuit
(b) Illustrates danger of simplification of circuit

LAYOUT DESIGN

There are many different layouts which can be used for a given circuit. In general, the optimum layout is that which uses the minimum area of silicon since this results in the highest production yield. However, it may be necessary to consider other factors, for example the number of crossovers which occur at a particular point in the circuit. As a guide to layout design a number of examples are given in this section. A shift register layout is used as an example to illustrate the calculation of the circuit capacitances.

Layout Examples

Figs. 16, 17 and 18 show three alternative layouts for a shift register stage driving a negator which is followed by a logic stage. The circuit diagram is shown in Fig. 15. The optimum layout depends on the type of circuit considered.

Calculation of Capacitances

The capacitance of a node to the substrate can be estimated by considering its components separately. These calculations are only approximate, but they do give a useful guide to the composition of the node capacitance. For a more detailed calculation it is necessary to consider the variation of thin oxide capacitance with voltage. Further details of this nature are available on application. The simplified equations used for estimating the node capacitance are as follows:

Capacitance of p-diffused regions to the substrate $= \dfrac{(\text{area in } \mu m^2)}{10(V+0{\cdot}7)^{\frac{1}{2}}}\,fF$,

where V = p-diffusion-to-substrate bias voltage.

Capacitance of aluminium over thick oxide to the substrate $= 3{\cdot}4 \times 10^{-2}\,(\text{area in } \mu m^2)\,fF$.

Capacitance of thin oxide to the substrate $= 3{\cdot}4 \times 10^{-1}\,(\text{area in } \mu m^2)\,fF$.

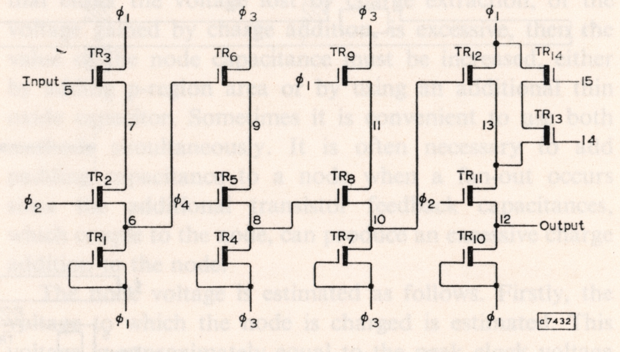

Fig. 15—Circuit diagram for layout examples

As an example the capacitance to the substrate for node 6 (Figs. 15 and 17) is estimated below. The diffusion bias voltage is taken as 10V. The source and drain of TR_6 are assumed to be connected to the substrate.

Area of diffusion as drawn $= (20\times20)+(20\times20)+10(34+26)$ $= 1400\mu m^2$.

Additional area due to sideways diffusion $= 649\mu m^2$.

Total capacitance of diffusion to substrate at −10V bias $= \dfrac{(1400+649)}{10(10{\cdot}7)^{\frac{1}{2}}} \simeq 63fF$.

Capacitance of aluminium over thick oxide to substrate $= 3{\cdot}4\times10^{-2}\times140 \simeq 4{\cdot}8fF$.

Capacitance of gate of TR_6 to substrate (aluminium over thin oxide) $= 3{\cdot}4\times10^{-1}\times12\times16 \simeq 65fF$.

Total capacitance of node 6 to substrate ($C_{6,0}$) $= 63+4{\cdot}8+65 \simeq 133fF$.

Although this calculation is very approximate it has been found that elementary calculations based on this value do give a useful guide to the circuit performance.

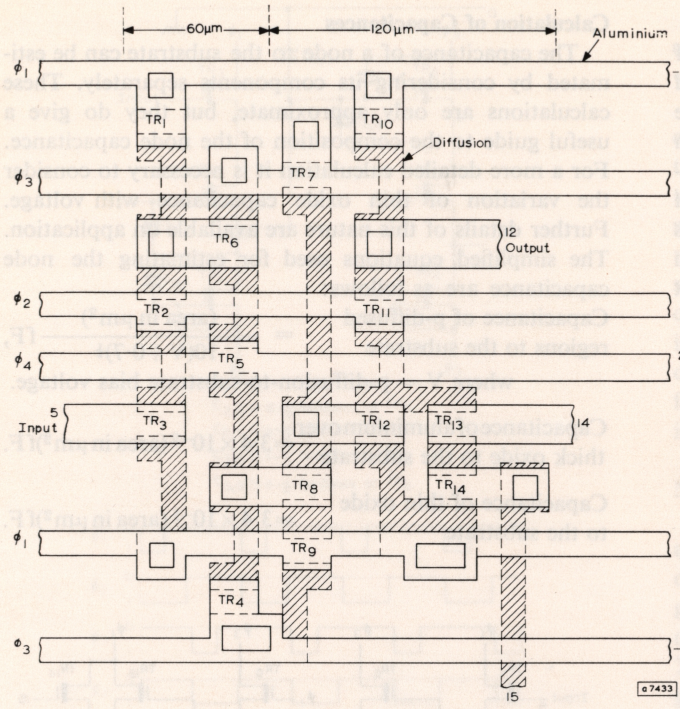

Fig. 16—Layout for four-phase circuits (Example 1)

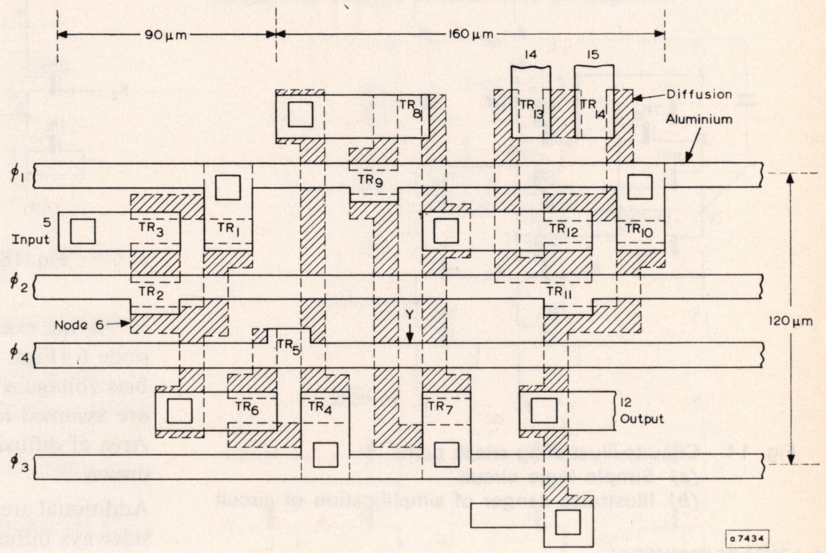

Fig. 17—Layout for four-phase circuits (Example 2)

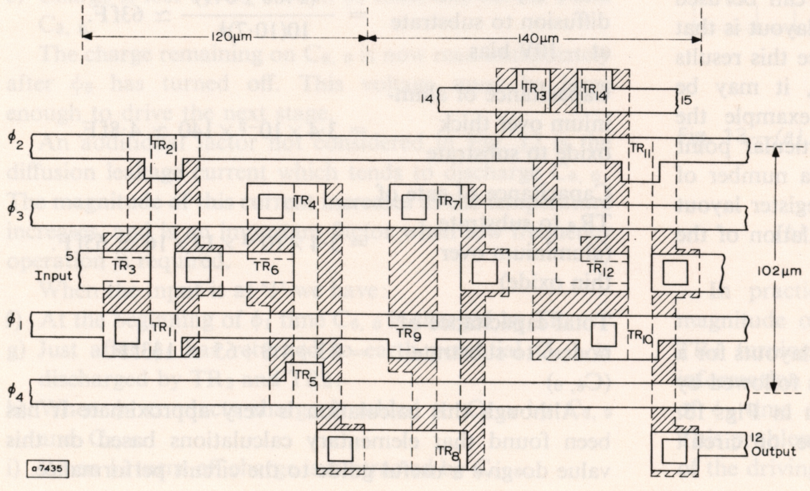

Fig. 18—Layout for four-phase circuits (Example 3)

The equations can be used to estimate crossover capacitances. In the layout of Fig. 17 the capacitance C_x between ϕ_4 and node 12 is given by:

$$C_x = 3{\cdot}4\times10^{-2} \text{ (p-region under the } \phi_4 \text{ line in } \mu\text{m}^2)\text{fF}$$
$$= 3{\cdot}4\times10^{-2}\times10\times13 \simeq 4{\cdot}4\text{fF}.$$

Transistor feedback capacitances can also be estimated. For example, the gate-to-drain capacitance C_{gd} of TR_6 in Fig. 17, when TR_6 is off, is given by:

$$C_{gd} = 3{\cdot}4\times10^{-1} \text{ (area gate overlaps drain in } \mu\text{m}^2)\text{fF}$$
$$= 3{\cdot}4\times10^{-1}\times12\times4{\cdot}5 \simeq 18\text{fF}.$$

Parasitic Channels

Parasitic channels can occur between two adjacent p-diffused regions if they are crossed by an aluminium interconnection. For example, a parasitic transistor can occur at Y in Fig. 17 with ϕ_4 serving as the gate. Normally the m-o-s transistor formed in this way has a thick gate oxide and consequently a high threshold voltage, which is normally greater than the maximum voltage rating of the circuit. However, parasitic channels may be formed which will destroy the circuit operation if this voltage rating is exceeded.

DESIGN METHODS

In this section a number of calculations which may assist the design are discussed. These calculations have been simplified and cannot be very accurate. For example, the diffusion leakage current which plays an important part in the circuit design cannot be precisely estimated. However, they do increase the understanding of the circuit operation.

Transient Analysis

The m-o-s transistor is a majority carrier device, and intrinsically has a very fast response time, usually a few nanoseconds. In a practical circuit the switching time is determined almost entirely by the time taken to charge and discharge the node capacitance; the time taken for the formation of the channel can be neglected.

The node capacitance charging time can be estimated from Appendix 1(A).

If we consider the node 6 in Figs. 15 and 17, the charging transistor TR_1 has a gain factor of about $6\mu A/V^2$. If $V_c = 25V$, $V_T' = 5V$ and $C_{6,0} = 130fF$ then the time taken for $C_{6,0}$ to charge to 18V is approximately:

$$\tau_{\text{ charge}} = \frac{2C_{6,0}}{\beta\Delta} = \frac{2\times130\times10^{-15}}{6\times10^{-6}\times(25-5-18)} \simeq 22\text{ns}.$$

The discharge time can be found approximately from the discharge time constant of $C_{6,0}$ as shown in Appendix 1(B). If we assume the capacitor is charged to 18V ($V_1 = 18V$), $V_{GE} = 15-5 = 10V$ and $\Delta = 2V$, then we have for node 6:

$$\tau_{\text{ discharge}} = \frac{C_{6,0}}{\beta V_{GE}}\log_e\frac{V_1(2V_{GE}-\Delta)}{\Delta(2V_{GE}-V_1)}$$
$$= \frac{130\times10^{-15}}{6\times10^{-6}\times10}\log_e\frac{18(20-2)}{2(20-18)}$$
$$= 10\text{ns}.$$

These calculations neglect the effect of source-substrate bias on threshold voltage.

Calculation of Charge Lost or Gained at a Node

In a complex layout charge is lost or gained at a node by transistor feedback capacitance. If that node feeds other transistors in the circuit then crossover capacitances may also alter the charge. It is important to assess after all the charge additions and extractions have occurred, that either:

a) If the output is at '1' a sufficient voltage remains at the time the output is read to drive the next stage.

or b) If the output is at '0' the voltage is less than the threshold voltage at the time it is read.

It is probably only necessary to perform this calculation for certain 'worst case' nodes which are revealed by a visual inspection.

Although it is necessary to perform both calculations for the critical nodes it is often found that (b) is the more difficult requirement. For example, in the shift register circuit of Fig. 12 the voltage added to node 6 (by $C_{6,9}$ and crossover capacitances) must be less than the threshold voltage of TR_6; this voltage V_A is indicated on the waveform of $C_{6,0}$. If the calculations for a node show that either the voltage lost by charge extraction, or the voltage gained by charge addition, is excessive, then the value of the node capacitance must be increased, either by adding p-region area or by using an additional thin oxide capacitor. Sometimes it is convenient to use both methods simultaneously. It is often necessary to add padding capacitance to a node when a fan-out occurs since the additional transistor feedback capacitances, which couple to the node, can produce an excessive charge addition to the node.

The node voltage is estimated as follows. Firstly, the voltage to which the node is charged is estimated. This voltage is approximately equal to the peak clock voltage minus the threshold voltage of the load m-o-s transistor; this threshold voltage will probably be a volt or two greater than the normal threshold voltage as the source of the load transistor is biased with respect to the substrate. Secondly, the transistor feedback and crossover capacitances which couple to the node are estimated from the layout as shown in *Calculation of Capacitances* (page 273). The magnitude of the node voltage reduction ΔV produced by these capacitances is given by:

$$\Delta V = \frac{1}{C}\,\Sigma_n C_n \Delta V_n.$$

At low operating frequencies the charge at a node lost by diffusion leakage current may be important. This loss of charge will be greatest at elevated temperatures as the diffusion leakage current increases with temperature. The area A of the node diffusion can be found from the layout and the leakage current I_c estimated from the equation:

$$I_c = K_1A, \text{ where } K_1 \text{ is a constant.}$$

As the leakage current is, to a first approximation, independent of the applied voltage, the voltage fall $\Delta V'$ in a time t due to leakage current is given by: $\Delta V' = I_ct/C$. Thus for node 6, Figs. 15 and 17, $A = 2049\mu m^2$, $C_{6,0} = 133fF$, K_1 at $85°C = 15pA/\mu m^2$ (say), so if $t = 25\mu s$ we have:

$$\Delta V' = \frac{15\times10^{-12}\times2049\times25\times10^{-6}}{133\times10^{-15}} \simeq 5{\cdot}8V.$$

It should be stressed that a wide production spread is to be expected for K_1 and that this calculation is for guidance only.

The layout must be checked to ensure that in each case reduction of node voltage is within the limits imposed by the circuit design. Fortunately only a few of the many nodes on a layout will be critical and experience and visual inspection will indicate these.

ACKNOWLEDGEMENT

The work described in this article has resulted partly from work carried out in conjunction with the Telephone Manufacturing Company Limited. The authors wish to record their appreciation of this contribution.

APPENDIX 1

(A) Node charging time

Fig. 19 shows the equivalent circuit and waveforms of a load m-o-s transistor charging a node capacitance.

As the transistor TR_1 is saturated,

$$i = \frac{\beta}{2}(V_i - v_0 - V_T)^2.$$

V_T varies during the transient but for simplicity assume it remains constant at its maximum value V_T'.

Hence,

$$\frac{dv_0}{dt} = \frac{\beta}{2C}(V_i - v_0 - V_T)^2.$$

Integrating,

$$\frac{\beta}{2C}\int_0^{\tau} dt = \int_0^{(V_i - V_T' - \Delta)} \frac{dv_0}{(V_i - v_0 - V_T')^2}$$

$$\frac{\tau\beta}{2C} = \frac{1}{\Delta} - \frac{1}{V_i - V_T'}.$$

If charging is nearly complete, that is $\Delta \ll (V_i - V_T')$, then,

$$\tau = \frac{2C}{\beta\Delta}.$$

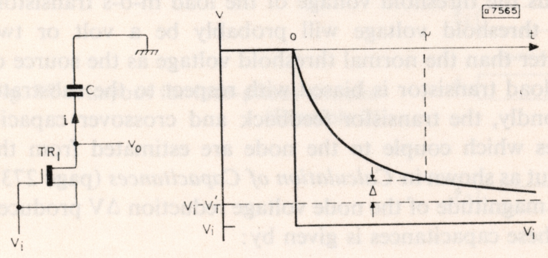

Fig. 19—Node capacitance charging time

(B) Node discharge time

Fig. 20 shows the equivalent circuit and waveforms of an m-o-s transistor discharging the node capacitance. As transistor TR_1 operates below the knee voltage,

$$i = \beta\left(v_0 V_{GE} - \frac{v_0^2}{2}\right),$$

where V_{GE} is effective gate voltage, $V_{GE} = V_G - V_T$.

Hence,

$$\frac{dv_0}{dt} = \frac{\beta}{C}\left(v_0 V_{GE} - \frac{v_0^2}{2}\right).$$

Integrating,

$$\frac{\beta}{C}\int_0^{\tau} dt = 2\int_{\Delta}^{V_i} \frac{dv_0}{v_0 2V_{GE} - v_0^2} = \frac{1}{V_{GE}}\int_{\Delta}^{V_i}\left(\frac{1}{v_0} + \frac{1}{2V_{GE} - v_0}\right)dv_0$$

$$\frac{\tau\beta}{C} = \frac{1}{V_{GE}}\log\left[\frac{v_0}{2V_{GE} - v_0}\right]_{\Delta}^{V_i}$$

$$\tau = \frac{C}{\beta V_{GE}}\log\left[\frac{V_i(2V_{GE} - \Delta)}{\Delta(2V_{GE} - V_i)}\right].$$

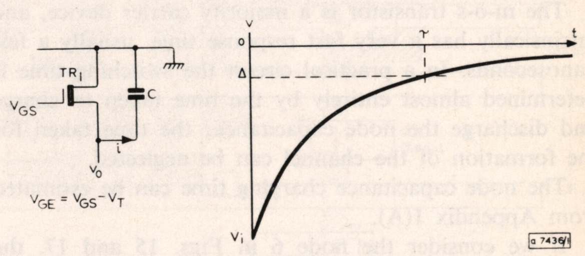

Fig. 20—Node capacitance discharging time

Dynamic Braking of D.C. Shunt Motors

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The theoretical aspects of dynamic braking are considered with reference to mechanical load and braking time. Equations are derived relating the principal variables to enable braking time and brake resistor values to be calculated. Practical circuits are given for simple dynamic braking and also braking associated with reversing and speed changing drives.

INTRODUCTION

In certain motor control applications it is necessary to apply braking during parts of the operating cycle. Several braking systems can be used, the choice depending upon the type of control required, and the permissible cost. The various systems can be classified into four groups:

1) Mechanical friction braking

2) Electromechanical, magnetic and eddy-current braking

3) Dynamic braking

4) Regenerative braking.

In the first two groups, the brake operates directly on the motor or load shaft and does not in any way depend on the motor for its operation. The method of operation is straightforward and easily understood, and such systems are relatively inexpensive in their simpler forms.

Dynamic braking uses the fact that a separately excited d.c. shunt wound motor can also be used as a generator. When braking, the motor generates current and drives it through a fixed resistive load; the energy thus dissipated produces the braking torque.

Regeneration braking is the most elegant system as it not only makes use of the generating property of the motor but, instead of wasting the braking energy in a static load, returns it to the supply. This method of braking is the most complex of the four groups, and is generally used only in large drives where economy of electrical energy is significant and the heat to be dissipated would be an embarassment, or where close control of deceleration is required. It is also sometimes used in fully controlled systems which include reversing, because the overall braking system design can be better integrated with the thyristor speed control. Generally a regenerative system will be more expensive than the other systems, and will be used only where its particular advantages can be fully realised.

This article considers in detail dynamic braking, because it is a method of braking which has a number of advantages over the mechanical systems without the complexity and cost of the regenerative system.

THEORETICAL ANALYSIS OF DYNAMIC BRAKING

When designing a braking system a number of parameters have to be considered. The most important of these is probably the time which will be required to stop the particular piece of machinery from a certain speed; that is, the braking time. To find the braking time the mechanical energy stored in the motor and its load can be equated with the energy dissipated in the brake, which in this case is the combined electrical loss in the motor armature resistance and the external braking resistor.

The total stored energy in the motor and its load is given by the equation

$$E_0 = \tfrac{1}{2}J \cdot \omega_0^2, \qquad \ldots(1)$$

where,

E_0 = Initial stored energy (joules)

J = Moment of inertia of motor and load (kg·m²)

ω_0 = Initial speed (rad/s).

At a reduced speed ω_1

$$E_1 = \tfrac{1}{2}J \cdot \omega_1^2. \qquad \ldots(2)$$

Therefore, if the motor speed is to be reduced from ω_0 to ω_1, the energy to be dissipated in the braking circuit is given by the equation

$$E_0 - E_1 = \tfrac{1}{2}J(\omega_0^2 - \omega_1^2). \qquad \ldots(3)$$

The energy dissipated in the braking circuit is given by the equation

$$E_b = \int_0^{t_1} i^2 \cdot R \cdot dt, \qquad \ldots(4)$$

where t_1 (in seconds) is the time to brake to speed ω_1,

R = total brake circuit resistance (in ohms), that is, motor armature resistance plus external brake resistance

i = armature current (in amperes).

If we now consider the motor as a generator, the open circuit armature voltage is a linear function of speed.

Thus,

$$v = V_0 \frac{\omega}{\omega_0} \qquad \ldots(5)$$

and

$$i = v/R \qquad \ldots(6)$$

where

V_0 = armature voltage at speed ω_0, and

v = armature voltage at speed ω.

Substitution in Eq. 4 gives,

$$E_b = \frac{V_0^2}{\omega_0^2 \cdot R} \int_0^{t_1} \omega^2 \cdot dt. \qquad \ldots(7)$$

Equating energies given by Eqs. 3 and 7 we have,

$$\tfrac{1}{2}J(\omega_0^2 - \omega_1^2) = \frac{V_0^2}{\omega_0^2 . R} \int_0^{t_1} \omega^2 \cdot dt, \qquad \ldots(8)$$

or

$$\frac{\omega_0^2 \cdot R \cdot J}{2V_0^2}(\omega_0^2 - \omega_1^2) = \int_0^{t_1} \omega^2 \cdot dt. \qquad \ldots(9)$$

Integrating and evaluating the constant gives,

$$t_1 = \frac{\omega_0^2 \cdot R \cdot J}{V_0^2} \cdot \log_e \left[\frac{\omega_0}{\omega_1}\right] \qquad \ldots(10)$$

In practice there will always be some additional braking produced by mechanical friction and windage. This may be conveniently taken into account by assuming that it may be represented by some effective braking resistor R_m which is always present. The error introduced by this assumption will be small when the mechanical braking effect is small compared with the electrical braking.

We can now write the total braking time T in terms of electrical braking and mechanical braking times. Thus,

$$\frac{1}{T} = \frac{1}{t_1} + \frac{1}{t_m}, \qquad \ldots(11)$$

where t_m is the time to reduce speed from ω_0 to ω_1 with no electrical braking connected.

If we make the assumption that,

$$t_m = \frac{\omega_0^2 \cdot R_m \cdot J}{V_0^2} \cdot \log_e \left[\frac{\omega_0}{\omega_1}\right] \qquad \ldots(12)$$

then for Eqs. 10, 11 and 12, we may write

$$\frac{1}{T} = \frac{V_0^2}{\omega_0^2 . J . \log_e \left[\frac{\omega_0}{\omega_1}\right]} \left[\frac{1}{R} + \frac{1}{R_m}\right] \qquad \ldots(13)$$

or

$$T = \frac{\omega_0^2 . J . \log_e \left[\frac{\omega_0}{\omega_1}\right]}{V_0^2} \left[\frac{R . R_m}{R + R_m}\right] \qquad \ldots(14)$$

DESIGN EQUATIONS AND PRACTICAL EXAMPLES

To make the theoretical equations more useful to the system designer some simplifying assumptions can be made and some guidance given on the evaluation of the remaining constants.

Many motors are supplied from the single phase 240V mains and have a maximum speed of 1500 rev/min. A motor of this type will have a rated armature voltage of about 170V and a back e.m.f. at full speed of about 160V. If we assume a speed reduction to 10% of top speed, then the braking time is given by Eq. 15.

$$T = 2{\cdot}22 . J \left[\frac{R . R_m}{R + R_m}\right]. \qquad \ldots(15)$$

The moment of inertia J, of the motor and its mechanical load, may be determined either by calculation or by measurement.

Let us consider a method of calculation first; a motor and its load can often be sub-divided into a number of solid concentric cylinders of approximately regular shapes.

For a solid cylinder of mass M and radius a, the moment of inertia in $kg \cdot m^2$ is

$$J = \tfrac{1}{2}Ma^2. \qquad \ldots(16)$$

For a number of such cylinders the total inertia is given by

$$J = J_1 + J_2 + \ldots\ldots + J_n. \qquad \ldots(17)$$

Alternatively, direct measurements may be used to derive J. The time taken for the motor to fall to 10% of its initial speed can be measured for two different values of braking resistor; we then have the equations

$$T_1 = 2{\cdot}22J \left[\frac{R_1 . R_m}{R_1 + R_m}\right] \qquad \ldots(18)$$

$$T_2 = 2{\cdot}22J \left[\frac{R_2 . R_m}{R_2 + R_m}\right]. \qquad \ldots(19)$$

From these we can obtain,

$$J = \frac{\left[\frac{1}{R_1} - \frac{1}{R_2}\right]}{2{\cdot}22\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}. \qquad \ldots(20)$$

Having now derived the value for J, we can then calculate R_m from Eq. 18 or R_m may be measured directly by timing the rate of deceleration of the motor without electrical braking and then using Eq. 12.

When all the system constants have been either calculated or measured it is possible, with the aid of Eq. 14 or Eq. 15, to calculate the value of braking resistor for any required rate of braking.

Examples

As an example we will consider the practical case of a 5 hp drive where $T_1 = 2s$ when R_1 was open circuit and $T_2 = 1{\cdot}2s$ when $R_2 = 6{\cdot}43\Omega$.

From Eq. 20,

$$J = \frac{1/6{\cdot}43}{2{\cdot}22\left(\frac{1}{1{\cdot}2} - \frac{1}{2}\right)} \qquad \ldots(21)$$

or

$$J = 0{\cdot}21 kg \cdot m^2.$$

Substitution in Eq. 12 gives,

$$R_m = 4{\cdot}25\Omega.$$

From Eq. 15 we then have,

$$T = 2{\cdot}22 \times 0{\cdot}21\left(\frac{4{\cdot}25R}{R + 4{\cdot}25}\right)s, \qquad \ldots(22)$$

or

$$T = 1{\cdot}98 \frac{R}{(R + 4{\cdot}25)} s. \qquad \ldots(23)$$

Measurements were made on a motor with the above data with a number of different values of brake resistor R. The measured values of T and calculated values of T obtained from Eq. 23 are tabulated below.

Value of R (Ω)	Measured T (s)	Calculated T (s)
6·43	1·2	1·195
3·43	0·8	0·875
1·33	0·55	0·475
0·88	0·4	0·34

It will be seen that agreement is quite good, particularly at the lower braking rates. Discrepancies at the high rates of braking may well be as much due to the difficulties associated with the time measurement as with the theoretical accuracy of the method.

In some applications the requirement is to stop the motor as quickly as possible and all that then needs to be estimated is the minimum safe value of brake resistor and the approximate braking time that can be achieved with it. Experience indicates that the minimum safe external braking resistor has a value equal to twice the armature resistance, giving a total circuit resistance equal to three times the armature resistance. We can also make certain general assumptions about the mechanical system if we assume that most of the inertia is supplied by the motor.

The moment of inertia of a cylinder of mass M and of radius a is given by

$$J = \tfrac{1}{2}Ma^2. \qquad \ldots(24)$$

For a cylinder of length L and density p:

$$M = \pi a^2 Lp. \qquad \ldots(25)$$

Therefore,

$$J = \frac{\pi}{2} . a^4 Lp. \qquad \ldots(26)$$

If we only consider motors with the same length to diameter ratio so that $L \propto a$, then

$$J = C_1 a^5, \qquad \ldots(27)$$

where C_1 is a constant.

The horsepower P of a motor of a given speed is approximately proportional to the armature volume. Thus,

$$P = C_2 a^3 \qquad \ldots(28)$$

where C_2 is a constant, and from Eqs. 27 and 28 we may write

$$J = C_3 P^{5/3} \qquad \ldots(29)$$

where C_3 is another constant.

Motor armature resistance is, in general, approximately inversely proportional to motor power, so that from Eqs. 15 and 29 the braking time T can be expressed as,

$$T = C_4 P^{2/3} \qquad \ldots(30)$$

where C_4 is a further constant.

As a guide to design, the constant C_4 may be taken to be about 0·16. Therefore, T (measured in seconds) is given approximately by

$$T = 0{\cdot}16P^{2/3} \qquad \ldots(31)$$

when the external braking resistance equals twice the armature resistance.

The energy to be dissipated during braking may be calculated by considering the energy stored in the rotating mechanical system before braking starts. Thus,

$$\text{mechanical stored energy} = \tfrac{1}{2}J . \omega_0^2 \text{ joules} \qquad \ldots(32)$$

If we again assume that the external braking resistance is twice the armature resistance, then two thirds of the stored energy is dissipated in the brake resistor, the remainder being dissipated in the armature. Therefore,

$$\text{Energy dissipated (joules) in the brake} = \tfrac{2}{3} \times \tfrac{1}{2} . J . \omega_0^2 \qquad \ldots(33)$$

$$= \tfrac{1}{3}J . \omega_0^2 \qquad \ldots(34)$$

The average wattage dissipated will depend upon the braking duty cycle, but the resistor selected must be capable of handling the peak energy even when the duty cycle would indicate a low power resistor.

In the case of the example quoted earlier, where $J = 0{\cdot}21 kg \cdot m^2$ and initial speed = 1500 rev/min,

$$\text{Energy} = \tfrac{1}{3} \times 0{\cdot}21 \times \left[\frac{2\pi \times 1500}{60}\right]^2$$

$$= 1575 \text{ joules.}$$

To summarise, the basic design equations are as follows: Braking time T, in seconds, is given by

$$T = \frac{\omega_0^2 . J . \log_e \left[\frac{\omega_0}{\omega_1}\right]}{V_0^2} \cdot \left[\frac{R . R_m}{R + R_m}\right].$$

$$\text{Braking energy} = \tfrac{1}{2}J(\omega_0 - \omega_1)^2 \text{ joules}$$

For a 1500 rev min motor supplied from 240V single phase mains, and for deceleration to 10% of initial speed:

$$T = 2{\cdot}22J \left[\frac{R . R_m}{R + R_m}\right].$$

COMBINED BRAKING SYSTEM WITH SPEED CONTROL SYSTEMS

The circuit design of dynamic braking systems has been considered so far with regard to the motor, mechanical load, and braking resistance required to produce a certain deceleration rate. Practical circuit configurations required to operate the braking system are now considered.

Two basic requirements must be satisfied in any braking system: the drive power to the motor must be interrupted before the braking resistor is connected, and the braking resistor must be disconnected before the drive power is reconnected. A secondary condition is that when the drive power is reconnected, it must be with the slow-start circuit and current limit fully operative as it will be a restart from zero speed. The connection of the brake resistor to the motor, and the logic required to interlock the braking and drive circuits, can be accomplished either with relays and contactors, or by solid state circuits and components. The choice will depend upon a number of factors such as relative cost, reliability requirements, ease of servicing and the user's personal preference. Many power engineers will be more familiar with relays and contactors, so a system based on these components will be described.

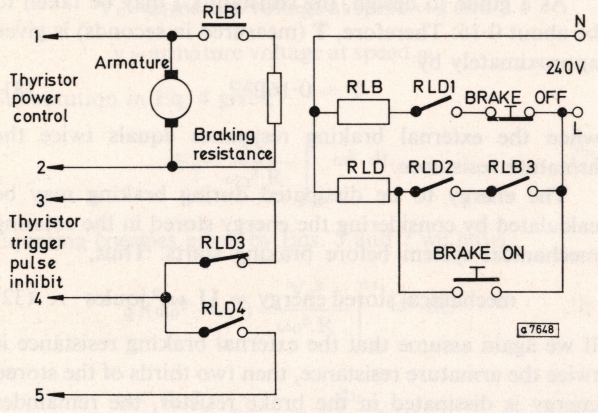
RLB1
1
N
Armature
Thyristor power control
240V
RLB
RLD1
BRAKE OFF
L
Braking resistance
2
3
RLD
RLD2
RLB3
Thyristor trigger pulse inhibit
RLD3
BRAKE ON
4
RLD4
5
a7648

Fig. 1—Dynamic braking circuit

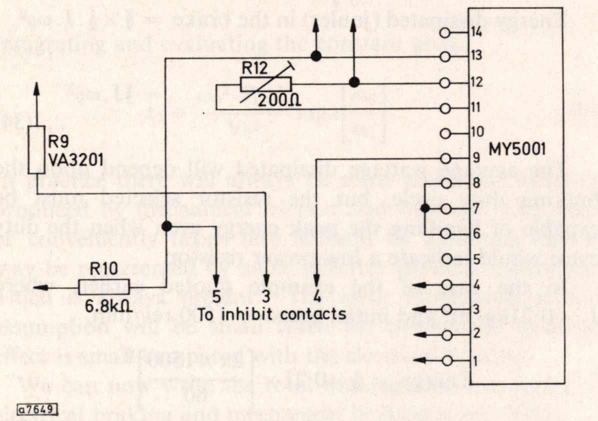
14
13
12
11
10
9
8
7
6
5
4
3
2
1
R12
200Ω
R9
VA3201
MY5001
R10
6.8kΩ
5
3
4
To inhibit contacts
a7649

Fig. 2—Connection of thyristor trigger pulse inhibit contacts of the braking system to the Mullard simple speed control system

The practical braking circuit shown in Fig. 1 is suitable for use with all Mullard thyristor speed control systems for d.c. shunt motors (Refs. 1, 2, 3 and 4). The basic mode of operation is the same for all circuits, the only difference being in the method of connection of the thyristor trigger pulse inhibit contacts. With some of the earlier circuits (Refs. 3 and 4) it is necessary to add a further transistor and a few additional components to provide facilities for trigger pulse inhibit and for immediate slow-start following rapid braking; all the more recent circuits and those in the course of preparation incorporate these additional facilities in the standard control system.

Operation of the BRAKE ON button (Fig. 1) energises relay RLD which opens contact RLD3 and closes RLD4 so that trigger pulses are prevented from reaching the thyristors in the power control circuit. After a delay of rather less than 10ms, the current in the motor armature will fall to zero. Operation of relay RLD also closes contact RLD1 which energises relay RLB. This is, in practice, a power contactor with contact RLB1 in series with the braking resistor. Its operating delay should be greater than 10ms, a condition normally satisfied by power contactors. If the contactor operating time is too short, it can be increased by using a d.c. coil with an RC slugging circuit, or by using magnetic slugging of the relay coil. Operation of RLB closes contact RLB1 to operate the brake, and contact RLB3 together with contact RLD2 form a hold-on circuit for relay RLD when the BRAKE ON button is released.

Operation of the BRAKE OFF button reverses this procedure by releasing relay RLB first to disconnect the braking resistor, followed by release of relay RL4D which restores trigger pulses to the thyristor.

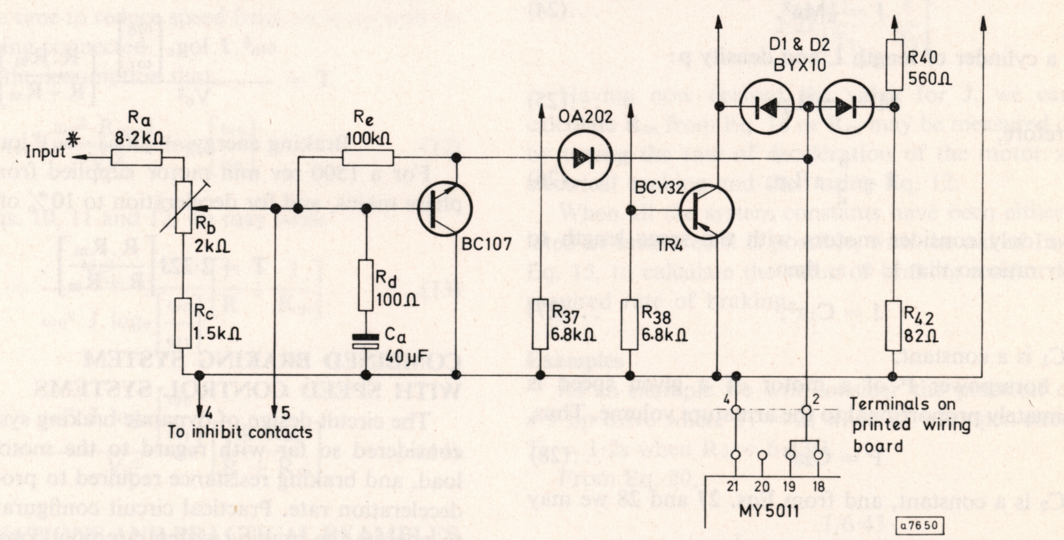
Input
*
Ra
8.2kΩ
Rb
2kΩ
Rc
1.5kΩ
Re
100kΩ
Rd
100Ω
Ca
40µF
BC107
OA202
BCY32
TR4
D1 & D2
BYX10
R40
560Ω
R37
6.8kΩ
R38
6.8kΩ
R42
82Ω
4
5
To inhibit contacts
1
2
Terminals on printed wiring board
21
20
19
18
MY5011
a7650

Fig. 3—Connection of thyristor trigger pulse inhibit contacts of the braking system to the Mullard tachometer speed control system and armature voltage feedback speed control system. *Input connected either to terminal 21 in the tachometer system (Ref. 4) or to point B in the armature voltage system (Ref. 3)

Fig. 2 shows the method of connection of the thyristor trigger inhibit contacts for the Mullard Simple System of motor speed control (Ref. 2), while Fig. 3 shows the corresponding connections for the Armature Voltage and Tachometer speed control systems (Refs. 3 and 4). A fast-response slow-start circuit is included in the circuit of Fig. 3 to give protection should the motor be restarted immediately after braking; this circuit forms part of all the more recent motor speed control circuits and will not have to be added in these cases.

In all cases the braking resistor is connected directly across the armature terminals of the motor. It should be remembered that this braking system depends for its operation upon the field of the motor being energised during the braking period.

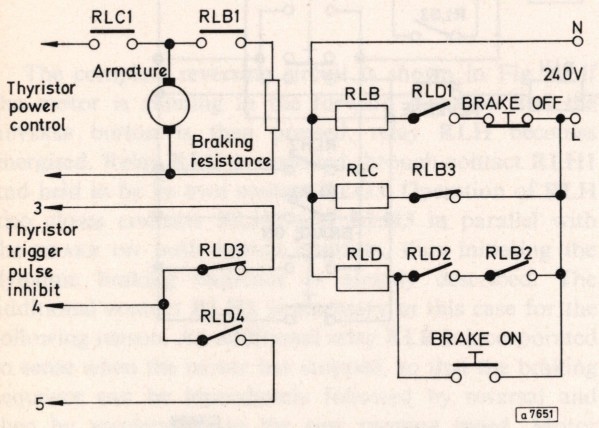
RLC1
RLB1
N
Armature
Thyristor power control
240V
RLB
RLD1
BRAKE OFF
L
Braking resistance
RLC
RLB3
3
Thyristor trigger pulse inhibit
RLD3
RLD
RLD2
RLB2
4
RLD4
BRAKE ON
5
a7651

Fig. 4—Alternative dynamic braking circuit

An alternative braking circuit is shown in Fig. 4. This incorporates a second power contactor RLC which has a contact RLC1 in series with the motor drive circuit. This contact opens before contact RLB1 closes and so provides double protection against the possibility of power being supplied to the motor while the brake resistor is connected. In low power drives, the contact RLC1 may be a normally-closed contact on relay RLB and a separate relay RLC will not then be required. The circuit of Fig. 5 shows how a dynamic braking system may be incorporated in a typical thyristor speed control circuit such as that of Ref. 3.

SOME OTHER CONTROL CIRCUITS UTILISING DYNAMIC BRAKING

The braking circuits described in the previous section can be used as the basis for several other types of control circuit. Two of these will be described here by way of example; they are a reversing circuit and a circuit for rapidly changing speed between two widely different levels.

Reversing Circuit

A contactor can be used to reverse a motor by changing over the connections to the motor armature. The dynamic braking circuit can be combined with the circuit which operates the reversing contactor to stop the motor before connecting power in the reverse direction. If the dynamic braking circuit which has been described above is used, the various thyristor trigger pulse inhibit and interlock circuits conveniently perform part of the reversing sequence. As the reversing contactor will not have to intercept the d.c. armature current, this is done by inhibiting trigger pulses to the thyristor; an a.c. type contactor can then be used, with considerable saving in cost and space.

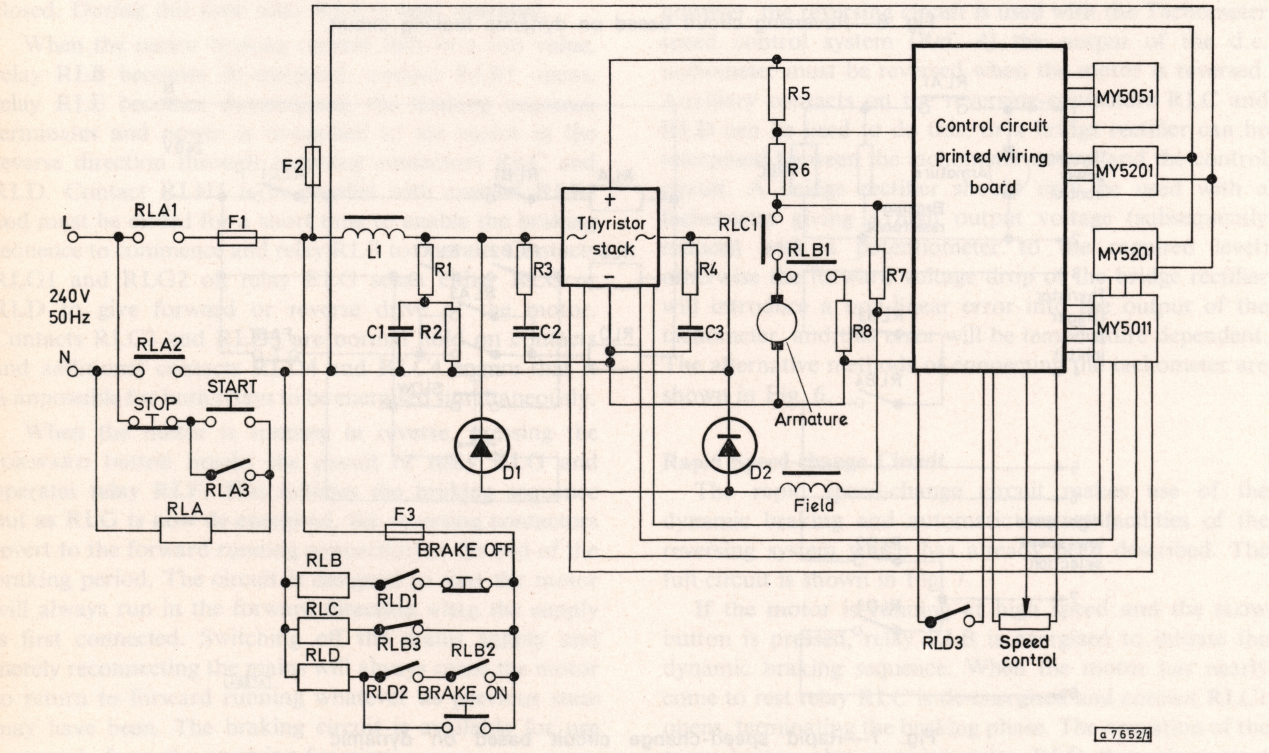
F2
RLA1
F1
L1
R1
R3
Thyristor stack
+
−
R4
RLC1
RLB1
R7
R5
R6
MY5051
MY5201
MY5201
MY5011
Control circuit printed wiring board
240V 50Hz
N
C1
R2
C2
C3
R8
Armature
RLA2
STOP
START
RLA3
D1
D2
Field
RLA
F3
BRAKE OFF
RLB
RLD1
RLC
RLB3
RLB2
RLD
RLD2
BRAKE ON
RLD3
Speed control
a7652

Fig. 5—Dynamic braking circuit for the armature voltage speed control system

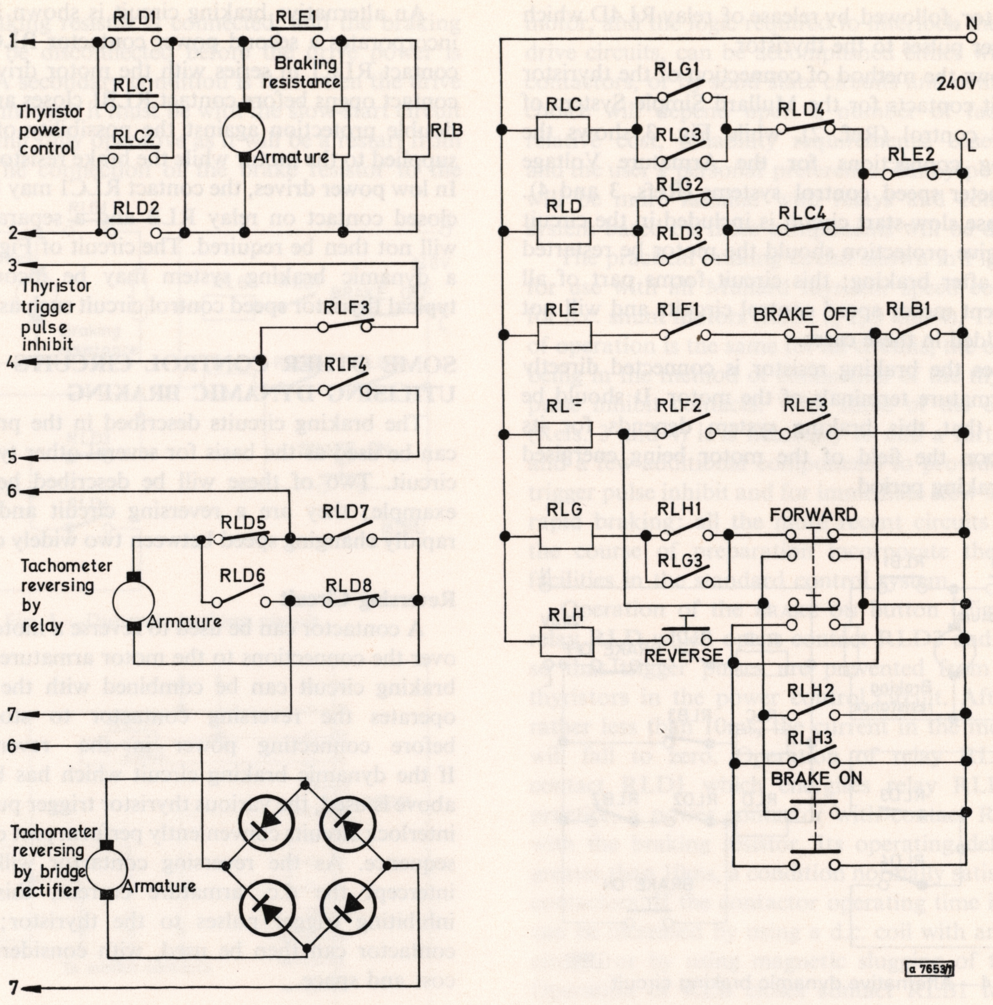
RLD1
RLE1
Braking resistance
RLC1
Thyristor power control
RLC2
Armature
RLB
RLD2
Thyristor trigger pulse inhibit
RLF3
RLF4
RLD5
RLD7
Tachometer reversing by relay
RLD6
RLD8
Armature
Tachometer reversing by bridge rectifier
Armature
1
2
3
4
5
6
7
6
7
N
240V
RLC
RLG1
RLC3
RLD4
RLE2
RLD
RLG2
RLD3
RLC4
RLE
RLF1
BRAKE OFF
RLB1
RLF
RLF2
RLE3
RLG
RLH1
FORWARD
RLG3
RLH
REVERSE
RLH2
RLH3
BRAKE ON
L
a7653

Fig. 6—Reversing circuit based on dynamic braking circuit

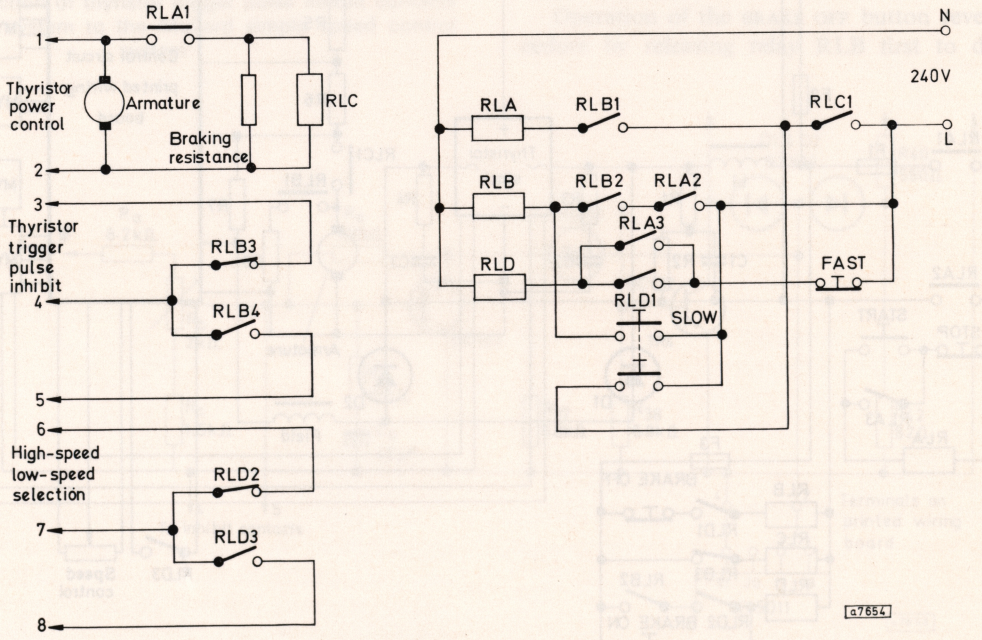
RLA1
Thyristor power control
Armature
RLC
Braking resistance
Thyristor trigger pulse inhibit
RLB3
RLB4
High-speed low-speed selection
RLD2
RLD3
1
2
3
4
5
6
7
8
N
240V
RLA
RLB1
RLC1
RLB
RLB2
RLA2
RLA3
RLD
FAST
RLD1
SLOW
L
a7654

Fig. 7—Rapid speed-change circuit based on dynamic braking circuit

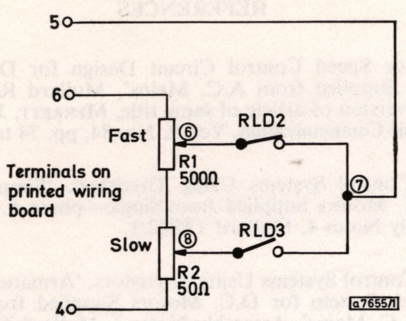
5
6
Fast
⑥
R1 500Ω
RLD2
⑦
Terminals on printed wiring board
Slow
⑧
R2 500Ω
RLD3
4
a7655

Fig. 8—Connection of the rapid speed-change circuit to the Mullard simple speed control system. The circled numbers refer to the terminal numbers in Fig. 7

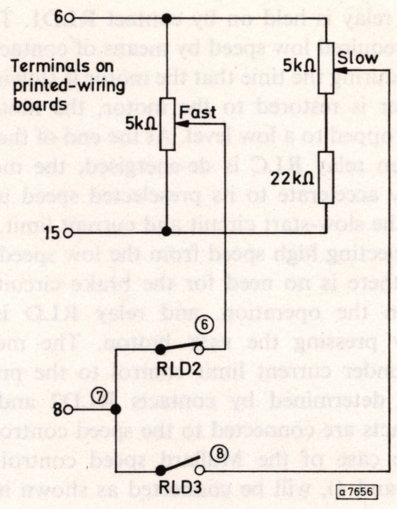
6
Terminals on printed-wiring boards
5kΩ
Slow
5kΩ
Fast
22kΩ
15
⑥
RLD2
8
⑦
⑧
RLD3
a7656

Fig. 9—Connection of the rapid speed-change circuit to the Mullard tachometer speed control system and armature feedback speed control system. The circled numbers refer to the terminal numbers in Fig. 7

The complete reversing circuit is shown in Fig. 6. If the motor is running in the forward direction and the REVERSE button is then pressed, relay RLH becomes energised. Relay RLG is operated through contact RLH1 and held in by its own contact RLG3. Operation of RLH also closes contacts RLH2 and RLH3 in parallel with the BRAKE ON push button contacts, thus initiating the dynamic braking sequence as already described. The additional contact RLH3 is necessary in this case for the following reason. An additional relay RLB is incorporated to sense when the motor has stopped, so that the braking sequence can be immediately followed by reversal and then by acceleration to the new running speed. Motor braking current holds RLB energised and contact RLB1 closed. During this time relay RLE is held operated.

When the motor braking current falls to a low value, relay RLB becomes de-energised, contact RLB1 opens, relay RLE becomes de-energised, the braking sequence terminates and power is re-applied to the motor in the reverse direction through reversing contactors RLC and RLD. Contact RLH3 is in parallel with contact RLB1 and must be closed for a short time to enable the braking sequence to commence and relay RLB to operate. Contacts RLG1 and RLG2 on relay RLG select either RLC or RLD to give forward or reverse drive ot the motor. Contacts RLC3 and RLD3 are normal hold on contacts and additional contacts RLD4 and RLC4 ensure that it is impossible for both relays to be energised simultaneously.

When the motor is running in reverse, pressing the FORWARD button breaks the circuit of relay RLG and operates relay RLF. This initiates the braking sequence but as RLG is now de-energised, the reversing contactors revert to the forward running connection at the end of the braking period. The circuit is designed so that the motor will always run in the forward direction when the supply is first connected. Switching off the mains supply and merely reconnecting the mains will always cause the motor to return to forward running whatever its previous state may have been. The braking circuit is available for use separately from the reversing function.

If this reversing circuit is used with the Mullard Simple Speed and Armature Voltage Control systems (Refs. 2 and 3), the reversing contacts RLC1 with RLC2 and RLD1 with RLD2 should be connected directly to the motor armature terminals. The armature voltage feedback circuit does not then need to be reversed as it is at all times connected directly to the thyristor bridge. When, however, the reversing circuit is used with the Tachometer speed control system (Ref. 4) the output of the d.c. tachometer must be reversed when the motor is reversed. Auxiliary contacts on the reversing-contactors RLC and RLD can be used to do this, or a bridge rectifier can be interposed between the tachometer output and the control circuit. A bridge rectifier should only be used with a tachometer giving a high output voltage (subsequently reduced with a potentiometer to the required level) otherwise the forward voltage drop of the bridge rectifier will introduce a non-linear error into the output of the tachometer, and this error will be temperature dependent. The alternative methods of connecting the tachometer are shown in Fig. 6.

Rapid Speed-change Circuit

The rapid speed-change circuit makes use of the dynamic braking and automatic restart facilities of the reversing system which has already been described. The full circuit is shown in Fig. 7.

If the motor is running at high speed and the SLOW button is pressed, relay RLB is energised to initiate the dynamic braking sequence. When the motor has nearly come to rest relay RLC is de-energised and contact RLC1 opens, terminating the braking phase. The operation of the SLOW button also energises relay RLD through contact

RLA3, the relay is held on by contact RLD1. This relay selects the required low speed by means of contacts RLD2 and RLD3 during the time that the motor is slowing down. When power is restored to the motor, the motor speed will have dropped to a low level. At the end of the braking period, when relay RLC is de-energised, the motor will immediately accelerate to its preselected speed under the control of the slow-start circuit and current limit.

When selecting high speed from the low speed running condition, there is no need for the brake circuit to take any part in the operation, and relay RLD is simply released by pressing the FAST button. The motor will accelerate under current limit control to the preselected high speed determined by contacts RLD2 and RLD3. These contacts are connected to the speed control circuits and, in the case of the Mullard speed control systems (Refs. 2, 3 and 4), will be connected as shown in Figs. 8 and 9.

REFERENCES

1. 'Thyristor Speed Control Circuit Design for D.C. Shunt Motors Supplied from A.C. Mains', Mullard Reprint Cr, revised version of article of same title, Merrett, J., **Mullard Technical Communication,** Vol. 9, No. 84, pp. 74 to 103.
2. Speed Control Systems Using Thyristors. 'Simple System for D.C. Motors Supplied from Single—phase A.C. Mains', Assembly Notes 4, Mullard TP922/1.
3. Speed Control Systems Using Thyristors. 'Armature-Voltage Feedback System for D.C. Motors Supplied from Single-phase A.C. Mains', Assembly Notes 3, Mullard TP921/1.
4. Speed Control Systems Using Thyristors, 'Tachometer System for D.C. Motors Supplied from Single-phase A.C. Mains', Assembly Notes 2, Mullard TP920/1.
5. Newell, A. F., Williamson, K. H., 'Regenerative Braking of D.C. Motors', **Mullard Technical Communications,** Vol. 8, No. 79, Jan. 1966, pp. 283 to 290.